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SAN FRANCISCO, CA 94105-2482

EXAMINER

SCHNEIDER, JOSHUA D

ART UNIT	PAPER NUMBER
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2182

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12

Please find below and/or attached an Office communication concerning this application or proceeding.



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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 09/740,669  
Filing Date: December 18, 2000  
Appellant(s): ROZARIO ET AL.

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Peter J. Yim  
For Appellant

**MAILED**

JUN 16 2004

Technology Center 2100

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 4/2/2004.

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**(1) *Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

**(2) *Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

**(3) *Status of Claims***

The statement of the status of the claims contained in the brief is correct.

**(4) *Status of Amendments After Final***

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) *Summary of Invention***

The summary of invention contained in the brief is correct.

**(6) *Issues***

The appellant's statement of the issues in the brief is correct.

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**(7) Grouping of Claims**

Appellant's brief includes a statement that claims 5-8 and 14-18 (Issue A), claim 9 (Issue B), and claims 1-4, 10-13, and 19-24 (Issue C), stand or fall together or alone as grouped, though without reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8). However, the claims are properly grouped to the issues.

**(8) Claims Appealed**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(9) Prior Art of Record**

5,504,919	Lee et al.	4-1996
6,052,375	Bass et al.	4-2000

**(10) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 5-8 and 14-18 are rejected under 35 U.S.C. 112, first paragraph. This rejection is set forth in a prior Office Action, mailed on 10/2/2003.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5 and 14, and claims 6-8 and 15-18 dependent from 5-14, are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it

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pertains, or with which it is most nearly connected, to make and/or use the invention.

The term "in-flight" is not established in the art, does not enable one of ordinary skill in the art to practice or understand the invention. An artisan would be unable to assign the "in-flight" field without further detail as to its definition.

Claim 9 is rejected under 35 U.S.C. 101. This rejection is set forth in a prior Office Action, mailed on 10/2/2003.

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 9 is rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. The shifting structure as taught by the invention could not be embodied as a FIFO device. A FIFO device by definition is processed in a very linear fashion. The first object added is the first object removed, not allowing for shifting, or sorting.

Claims 1-4, 10-13, and 19-24 are rejected under 35 U.S.C. 103(a). This rejection is set forth in a prior Office Action, mailed on 10/2/2003.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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Claims 1-4, 10-13, and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,504,919 to Lee et al. in further view of U.S. Patent 6,052,375 to Bass et al. With regards to claim 1, Lee teaches a shift structure having a plurality of entries, and a comparison logic circuit to sort the entries based on their respective weights (see abstract and Fig. 2). Lee does not teach the plurality of entries having a plurality of fields, or the entries being DMA channels. Bass teaches a scheduler for DMA channels data transfer. Bass teaches a plurality of fields in a parameter table (column 4, line 46, through column 5, line 38). Bass further teaches that queues are sorted for output to a traffic queue allocation manager (column 5, lines 42-44). Bass further teaches the DMA bus arbitration based on a straight priority fashion (column 5, lines 60-64). While Bass does not use the term weights, it is would have been obvious to one of ordinary skill in the art at the time of invention, that the terms weight and priority are interchangeable in this context. Both words, as used in this application, indicate an importance or superiority in relation to competing entities. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the DMA scheduler with the shift structure of Lee, in order to increase the speed of arbitration by increasing sorting efficiency.

With regards to claims 10 and 19, Lee teaches the writing of a plurality of entries into a shift structure, and a comparison logic circuit to sort the entries based on their respective assigned weights (see abstract and Fig. 2). Lee does not teach the plurality of entries having a plurality of fields, or the entries being DMA channels. Bass teaches a scheduler for DMA channels data transfer. Bass teaches a plurality of fields in a parameter table (column 4, line 46, through column 5, line 38). Bass further teaches that

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queues are sorted for output (column 5, lines 42-44). Bass further teaches the DMA bus arbitration selection based on a straight priority fashion (column 5, lines 60-64). It is inherent in Bass that the highest priority entry is read out for service (column 5, line 65, through column 6, line 2). With further regards to claim 19, it is inherent in Bass that all channels would be resorted after service as long as there is pending data. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the DMA scheduler with the shift structure of Lee, in order to increase the speed of arbitration by increasing sorting efficiency.

With regards to claim 11, it is inherent in Bass that all channels would be resorted after service as long as there is pending data.

With regards to claim 2, Lee teaches the comparison of the entry, or item, for insertion with the sorted entries in the shift structure (column 3, lines 5-8).

With regards to claims 3, 12, and 20, Lee teaches the entry being inserted, or written, behind the sorted entries with higher weights and shifting of entries in the shift structure with lower weights (Fig. 1b, and column 3, lines 13-18).

With regards to claims 4, 13, and 21, Lee teaches the entries having a plurality of fields (Fig. 2), and Bass teaches the entries being made of a plurality fields each assigned to a set of bits (column 4, line 46, through column 5, line 38).

With regards to claim 22, Bass teaches a priority field (column 5, lines 25-38), and it would have been obvious to one of ordinary skill in the art that a priority field would have a plurality of priority levels, as any binary field would have at least two levels.

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With regards to claims 23 and 24, SONET is an interface standard that is well known, and OC numbers are well known in the art. It would have been obvious to one of ordinary skill in the art that a priority field could be set according to OC numbers as bandwidth prioritizing is well known in the art.

**(11) Response to Argument**

Issue A - Rejection of claims 5-8 and 14-18 under 35 U.S.C. 112, first paragraph

Appellant has asserted the notion that a packet can be in-flight and yet be scheduled in the DMA is consistent in view of the specification. The term in-flight is described on page 14, lines 20-22 of the specification. It states, "a packet is considered to be in-flight when the packet is being processed, such as if a packet is being read out of memory, being sent out onto the bus, and the like." This was interpreted as saying that a packet is being "in-flight" when it is being transferred somewhere in order to fulfill some request.

With regards to this application, a shift structure and comparison logic are used to sort a plurality of entries corresponding to channels to be scheduled, based on their respective weights. Each of the entries has a plurality of fields that are used to determine a weight. According to claims 5 and 14, an in-flight field is to be used as one of the fields in the weight.

The first question is whether a packet that is sitting in a queue, waiting to be scheduled for DMA transfer is in fact in-flight. It can be interpreted that the packet has already been transferred from somewhere and is therefore in the middle of the process of being transferred to somewhere else, and is therefore in-flight. In this manner, all packets



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*waiting* to be scheduled for transmission would be interpreted to be in-flight for the current application. Alternatively, one could view could view that the term in-flight applies to only data actually being transmitted, and that the data which is sitting in a queue, waiting to be scheduled for transmission is not in-flight. In either case all of the entries waiting to be scheduled by the shift structure would have the same value in their in-flight fields. Appellant has in the appeal brief made clear that packets waiting to be scheduled for DMA transfer are in fact considered to be in-flight (page 5, paragraph 2).

There is, however, a second question. In order to sort a group of objects linearly, in this case DMA channel packets in ascending or descending weight, one would choose a number of criteria to differentiate the objects of that group. One would not choose a quality that all members of that group would either have or all not have. That is, if one was to sort a group of different types of apples into a line, one would not decide to shift all of the oranges to the back of the line and all of the apples to the front. When there are no oranges to be shifted, the operation of shifting oranges is never useful. Similarly, sorting based on an in-flight field, which all entries would have to comprise the same value; no entry would ever be shifted. Therefore, there is nothing in the specification to enable one of ordinary skill in the art to understand or practice the invention in a logical or useful manner. While appellant has in the appeal brief, given a set definition, there is still nothing that defines the term in-flight in a way that enables one of ordinary skill in the art in a practicable useful manner.

Issue B - Rejection of claim 9 under 35 U.S.C. 101

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Claim 9 includes the limitation, “wherein said shifting structure is a First-In First-Out (FIFO) device.” By definition, a FIFO is a type of queue, in which the data that is first in is the first data to be taken out, therefore First-In First-Out. Appellant has asserted that the comparison logic can be used to sort the data in the FIFO.

Appellant has failed to address the rejection in any manner. Examiner does not disagree that comparison logic can be used to sort a variety of entries in some sort of memory device. It is only asserted that once any shifting of sorted entries occurs, the device ceases to be a FIFO. A FIFO can best be compared to a pipe. If one were to place a series marbles just small enough to fit inside the pipe into a pipe, the marbles would come out of the other end in the same order that they were placed inside. Appellant has previously argued in Amendment A, received 8/11/2003, that as long as the data eventually gets out, the device is still a FIFO (pages 14 and 15). This is not at all the case. The name First-In First-Out precludes a First-In Eventually-Out ordering that Appellant requires in order to have a shift-sorting device.

Issue C - Rejection of claims 1-4, 10-13, and 19-24, under 35 U.S.C. 103(a)

With regards to claims 1, 10, and 19, Appellant has again failed to address the rejection. The only argument to the rejection under 35 U.S.C. 103(a) is made in the third line of page 7 of the Appeal Brief. Appellant states that parameters, of the Bass reference (as shown in Figure 8), used for deciding the priorities are not related to the entries of the queues but to the queues themselves. It is not clear what supposed difference is being shown by this remark, as that is precisely what the Appellant claims. The independent claims 1, 10, and 19, all include a limitation claiming shifting entries *corresponding to*

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*the multiple channels*, not corresponding to the data (or entries) in these channels (or queues). There is no argument to the combination of the references. There is no argument to the motivational statement.

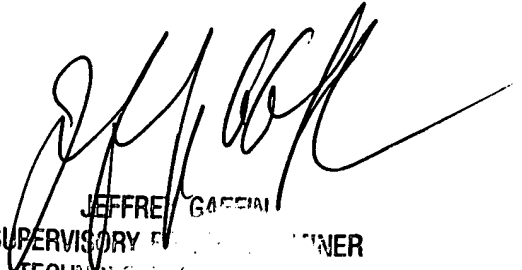
For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

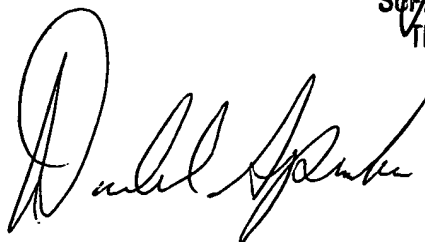
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